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IN THE CLAIMS

Presented below is a complete listing of the claims.

1. (Currently amended) A cache comprising:

a plurality of arrays of memory cells, the arrays being arranged in banks, each bank including regular arrays and a redundant array;

a bus having sets of data lines for connection to the regular arrays and to said redundant array; and

circuitry to connect a regular array to either a first set or a second set of the data lines, or to disconnect the regular array from the bus.

2. (Original) The cache of claim 1 wherein the circuitry comprises a bit that, when set to a first logic state, causes the circuitry to disconnect the regular array from the bus.

3. (Original) The cache of claim 2 wherein the circuitry is further operative to connect the redundant array to the bus responsive to the bit being set.

4. (Original) The cache of claim 1 wherein the arrays in a bank are arranged linearly.

5. (Original) The cache of claim 1 wherein the arrays in a bank are arranged in multiple rows.

6. (Original) The cache of claim 2, further comprising:
a plurality of repeaters each of which provides for series connection of an array with a data line of the bus.

7. (Currently amended) A cache, comprising:
a plurality of arrays of memory cells, the arrays being arranged in banks, each bank including regular arrays, A_{0-N}, and a redundant array;
a data bus having sets of N sets of bus lines, B_{0-N}, for connection to the regular arrays and to said redundant array;
logic associated with each array, the logic being configured with a bit that is set to a first state to connect an ith regular array to an ith set of the bus lines, with the redundant array being disconnected from the data bus; and
a change in the bit setting from the first state to a second state causing the regular array, Ai, to be disconnected from the data bus and the redundant array to be connected to the data bus.

8. (Original) The cache of claim 7 wherein the arrays in a bank are arranged linearly, regular arrays, A_0 to $A_{(i-1)}$ connect to bus lines B_0 to $B_{(i-1)}$, respectively, and regular arrays, $A_{(i+1)}$ to A_N connect to bus lines B_i to $B_{(N-1)}$, respectively, responsive to the change.

9. (Original) The cache of claim 7 wherein the arrays in a bank are arranged in multiple rows.

10. (Currently amended) The ~~A~~ cache of claim 7 wherein the logic includes a fuse circuit having a fuse, when the fuse is in a first conductivity state, the bit setting corresponding to the first state, and when the fuse is in a second conductivity state, the bit setting corresponding to the changed state.

11. (Original) The cache of claim 10, further comprising a plurality of repeaters each of which provides for series connection of an array with a data line of the bus.

12. (Currently amended) A method of operation for a cache, comprising:

changing a single bit associated with a cache bank from a first to a second logic state, the cache bank comprising a plurality of arrays of memory cells, the arrays including regular arrays, A_{0-N}, and a redundant array, the regular arrays being connected to corresponding bus lines, B_{0-N}, of a data bus when the single bit is in the first logic state;

disconnecting a regular array, A_i, from the data bus data bus responsive to the single bit state being changed to the second logic state; and

connecting the redundant array to the data bus responsive to the single bit state being changed to the second logic state.

13. (Original) The method of claim 12 wherein the data bus is unaffected by the single bit state being changed to the second logic state.

14. (Original) The method of claim 12 wherein changing the single bit state comprises blowing a fuse.

15. (Original) The method of claim 12 wherein the cache bank further comprises a plurality of repeaters each of which provides for series connection of an array with a data line of the data bus.